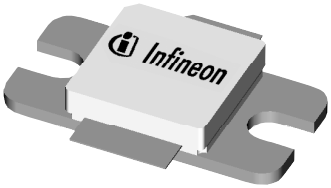
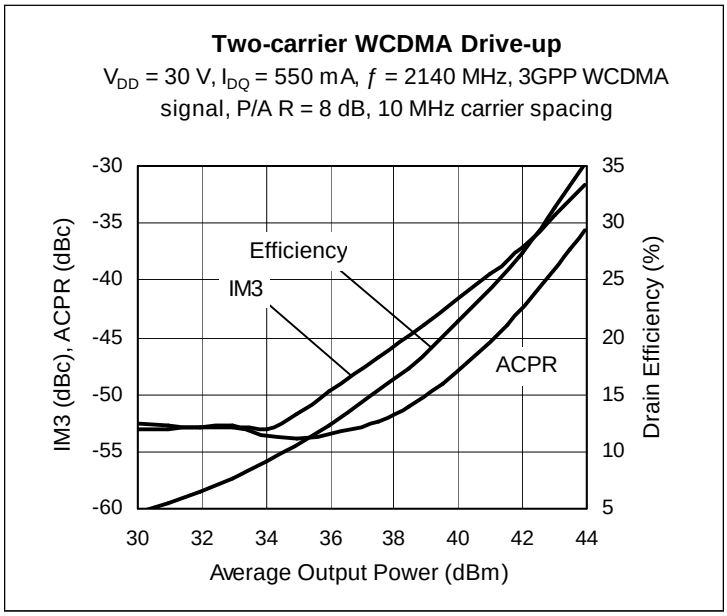
Thermally-Enhanced High Power RF LDMOS FET
70 W, 2110 – 2170 MHz

Description

The PTFA210701E is a thermally-enhanced, 70-watt, internally-matched *GOLDMOS*® FET intended for WCDMA applications. It is characaterized for single- and two-carrier WCDMA operation from 2110 to 2170 MHz. Thermally-enhanced packaging provides the coolest operation available. Full gold metallization ensures excellent device lifetime and reliability.



PTFA210701E
Package H-30265-2



Features

- Thermally-enhanced packages, Pb-free and RoHS-compliant
- Broadband internal matching
- Typical two-carrier WCDMA performance at 2140 MHz, 30 V
  - Average output power = 42 dBm
  - Linear Gain = 16.5 dB
  - Efficiency = 27.0%
  - Intermodulation distortion = –37 dBc
  - Adjacent channel power = –42.5 dBc
- Typical CW performance, 2170 MHz, 30 V
  - Output power at P–1dB = 80 W
  - Efficiency = 58%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 30 V, 70 W (CW) output power

RF Characteristics

WCDMA Measurements (tested in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 550 mA, P_{OUT} = 18 W average
f_1 = 2135 MHz, f_2 = 2145 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15.5	16.5	—	dB
Drain Efficiency	η_D	28	29	—	%
Intermodulation Distortion	IMD	—	–36.5	–35.5	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 30 V, I_{DQ} = 550 mA, P_{OUT} = 70 W PEP, f = 2140 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	16.5	—	dB
Drain Efficiency	η_D	—	41	—	%
Intermodulation Distortion	IMD	—	–29.5	—	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.125	—	Ω
Operating Gate Voltage	V_{DS} = 30 V, I_{DQ} = 550 mA	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	190	W
Above 25°C derate by		1.09	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 70 W CW)	$R_{\theta JC}$	0.92	°C/W

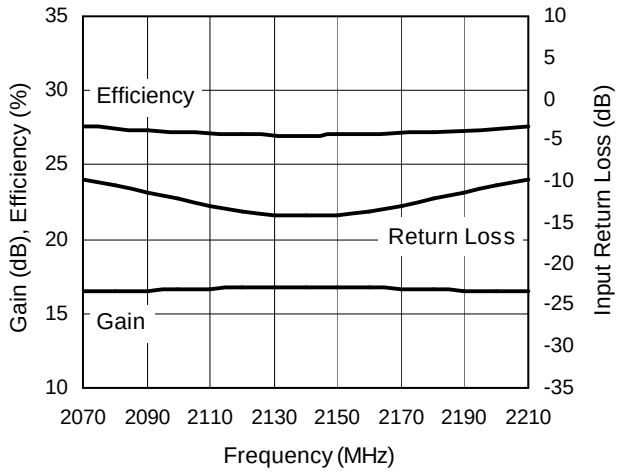
Ordering Information

Type and Version	Package Outline	Package Description	Marking
PTFA210701E V1	H-30265-2	Thermally-enhanced slotted flange, single-ended	PTFA210701E

Typical Performance (data taken in a production test fixture)

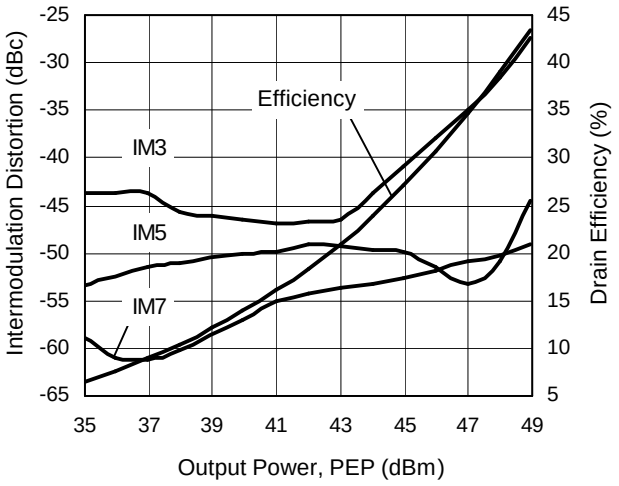
Broadband Performance

V_{DD} = 30 V, I_{DQ} = 550 mA, P_{OUT} = 42.5 dBm



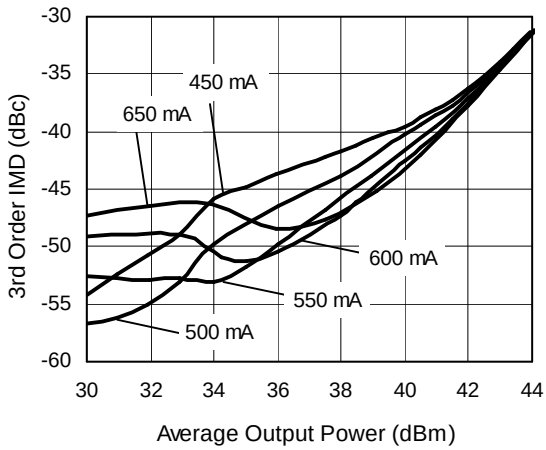
Two-tone Drive-up at Optimum I_{DQ}

V_{DD} = 30 V, I_{DQ} = 550 mA,
f = 2140 MHz, tone spacing = 1 MHz



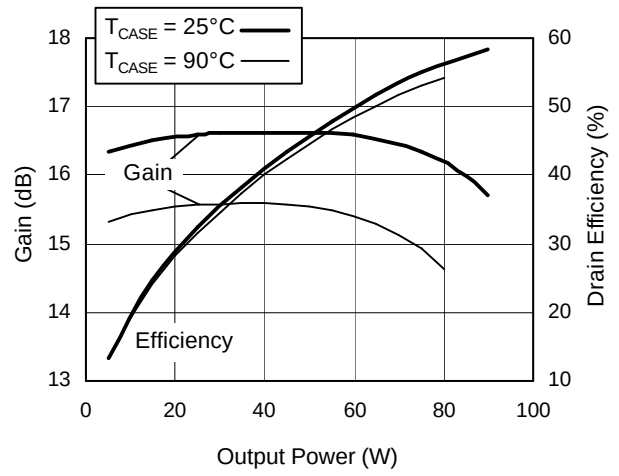
Two-carrier WCDMA at Selected Biases

V_{DD} = 30 V, f = 2140 MHz, 3GPP WCDMA signal,
P/AR = 8 dB, 10 MHz carrier spacing, series show I_{DQ}



Power Sweep, CW Conditions

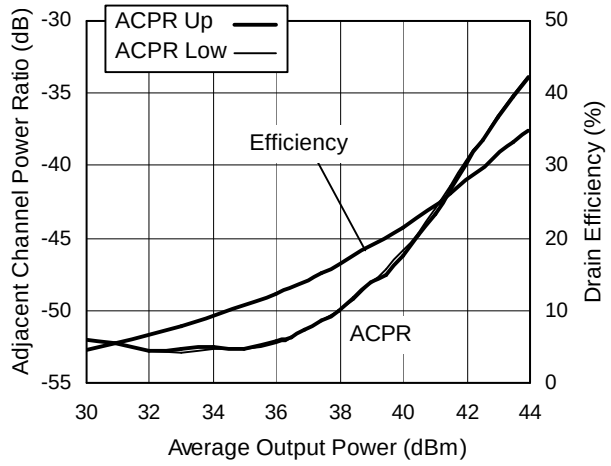
V_{DD} = 30 V, I_{DQ} = 550 mA, f = 2170 MHz



Typical Performance (cont.)

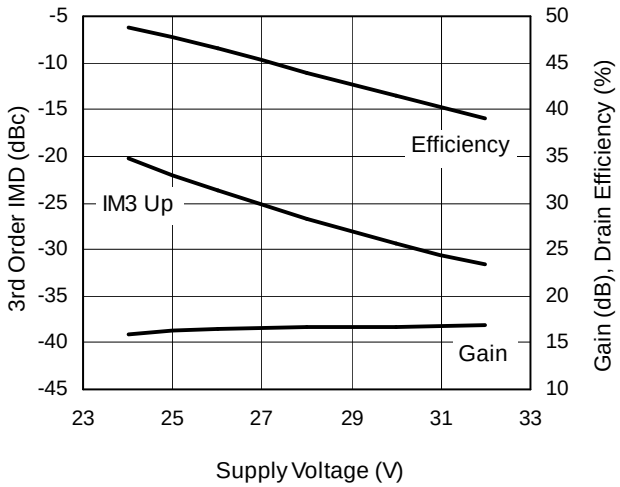
Single-carrier WCDMA Drive-up

V_{DD} = 30 V, I_{DQ} = 550 mA, f = 2140 MHz,
3GPP WCDMA signal, TM1 w/16 DPCH, 67% clipping,
P/A R = 8.5 dB, 3.84 MHz BW



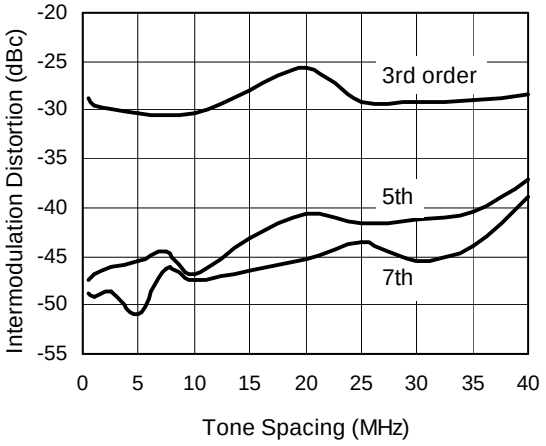
Voltage Sweep

I_{DQ} = 550 mA, f = 2140 MHz,
tone spacing = 1 MHz, P_{OUT} (PEP) = 48.5 dBm



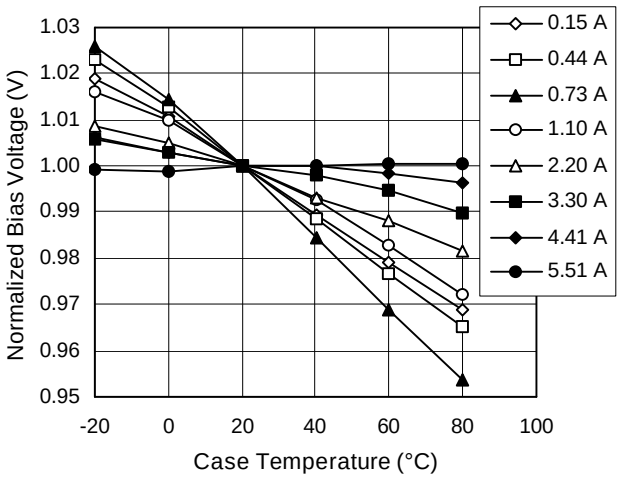
Intermodulation Distortion Products vs. Tone Spacing

V_{DD} = 30 V, I_{DQ} = 550 mA, f = 2140 MHz,
P_{OUT} = 48.5 dBm PEP

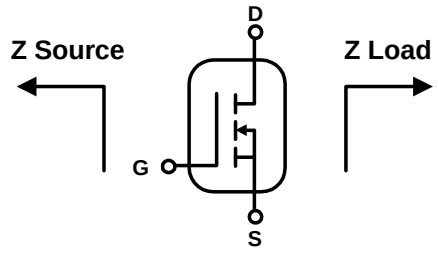


Bias Voltage vs. Temperature

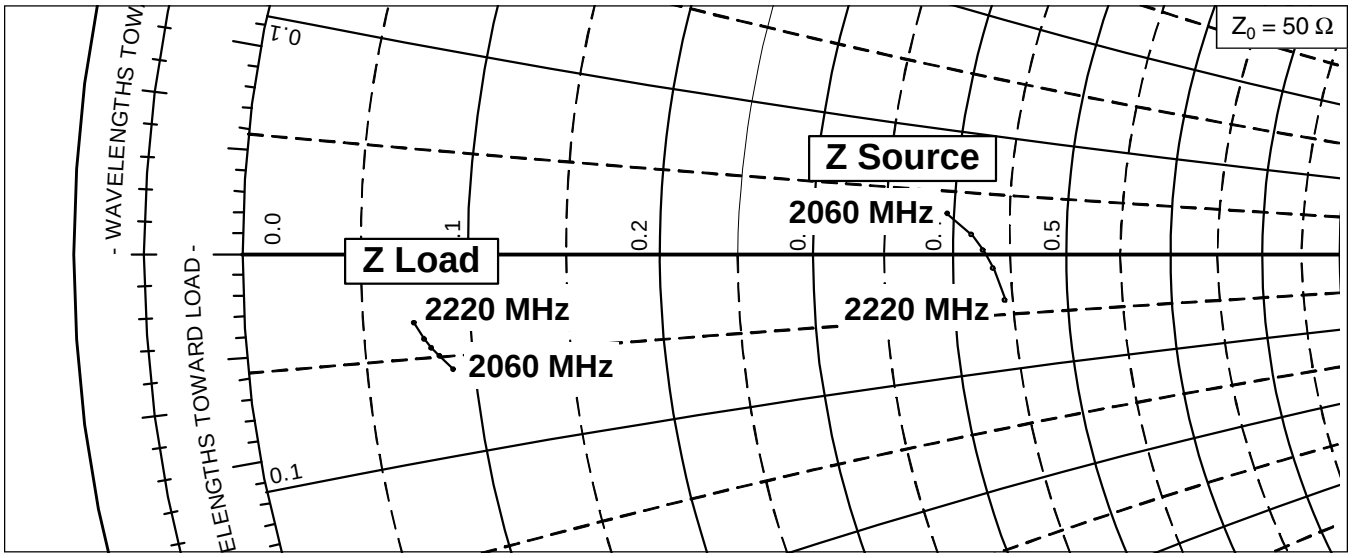
Voltage normalized to typical gate voltage,
series show current



Broadband Circuit Impedance

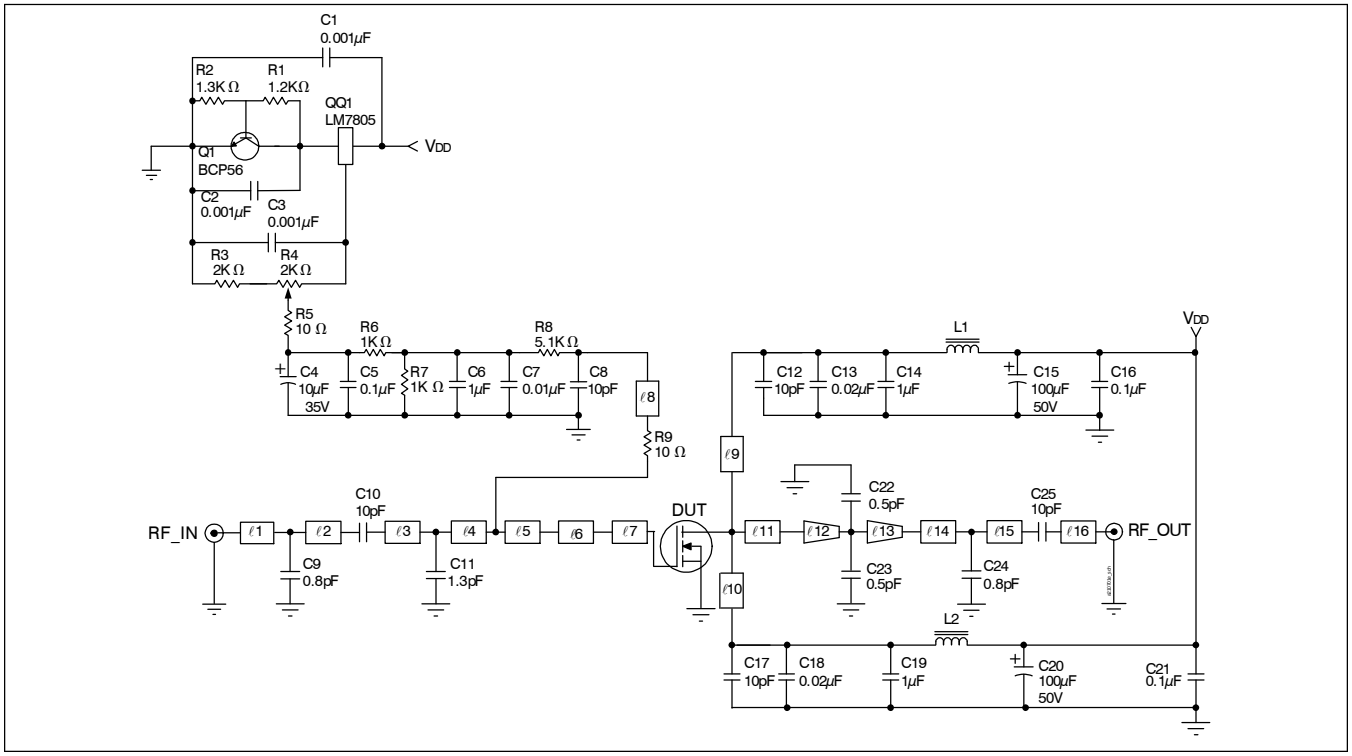


Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
2060	19.94	1.61	4.50	–2.87
2110	20.94	0.77	4.20	–2.50
2140	21.41	0.11	4.02	–2.29
2170	21.83	–0.69	3.88	–2.07
2220	22.26	–2.09	3.66	–1.66



See next page for circuit information

Reference Circuit



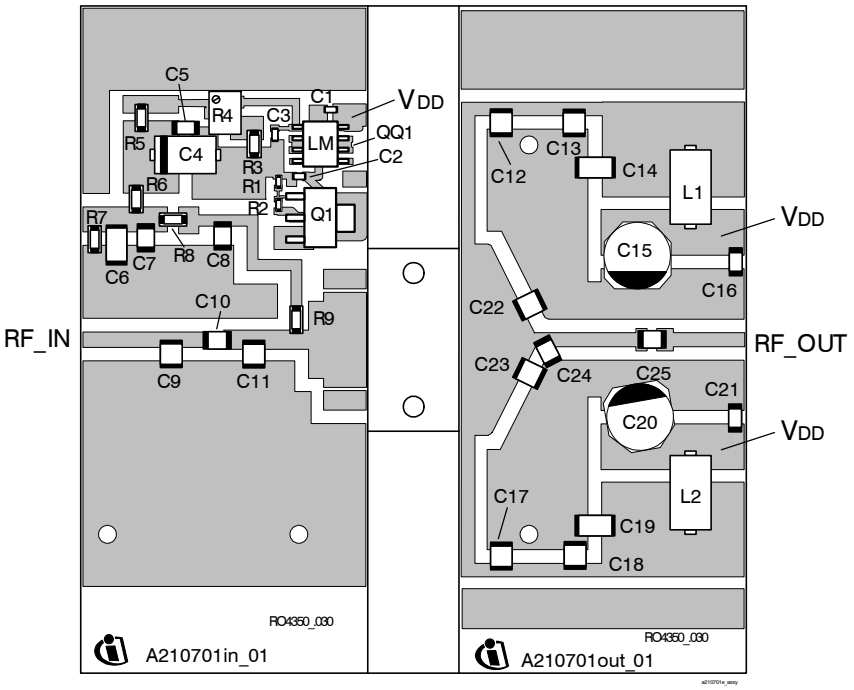
Reference circuit schematic for ƒ = 2140 MHz

Circuit Assembly Information			
DUT	PTFA210701E	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 3.48	Rogers 4350	1 oz. copper

Microstrip	Electrical Characteristics at 2140 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.112 λ, 50.0 Ω	9.53 x 1.78	0.375 x 0.070
ℓ2	0.053 λ, 50.0 Ω	4.52 x 1.78	0.178 x 0.070
ℓ3	0.044 λ, 43.0 Ω	3.73 x 2.18	0.147 x 0.086
ℓ4	0.054 λ, 43.0 Ω	4.57 x 2.18	0.180 x 0.086
ℓ5	0.016 λ, 43.0 Ω	1.37 x 2.18	0.054 x 0.086
ℓ6	0.022 λ, 14.6 Ω	1.73 x 8.76	0.068 x 0.345
ℓ7	0.062 λ, 12.2 Ω	4.88 x 10.82	0.192 x 0.426
ℓ8	0.214λ, 61.0 Ω	18.36 x 1.22	0.723 x 0.048
ℓ9, ℓ10	0.211 λ, 50.0 Ω	17.91 x 1.57	0.705 x 0.062
ℓ11	0.042 λ, 6.5 Ω	3.25 x 21.84	0.128 x 0.860
ℓ12 (taper)	0.043 λ, 6.5 Ω / 16.2 Ω	3.30 x 21.84 / 7.80	0.130 x 0.860 / 0.307
ℓ13 (taper)	0.023 λ, 16.2 Ω / 50.0 Ω	1.88 x 7.80 / 1.57	0.074x 0.307 / 0.062
ℓ14	0.010 λ, 50.0 Ω	0.89 x 1.57	0.035 x 0.062
ℓ15	0.130 λ, 50.0 Ω	11.07 x 1.57	0.436 x 0.062
ℓ16	0.116 λ, 50.0 Ω	9.88 x 1.57	0.389 x 0.062

[1]Electrical characteristics are rounded.

Reference Circuit (cont.)



*Reference circuit assembly diagram (not to scale)**

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 µF, 35 V	Digi-Key	399-1655-2-ND
C5, C16, C21	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6, C14, C19	Ceramic capacitor, 1 µF	Digi-Key	445-1411-2-ND
C7	Capacitor, 0.01 µF	ATC	200B 103
C8, C10, C12, C17, C25	Ceramic capacitor, 10 pF	ATC	100B 100
C9, C24	Ceramic capacitor, 0.8 pF	ATC	100B 0R8
C11	Ceramic capacitor, 1.3 pF	ATC	100B 1R3
C13, C18	Capacitor, 0.02 µF	ATC	200B 203
C15, C20	Electrolytic capacitor, 100 µF, 50 V	Digi-Key	PCE3718CT-ND
C22, C23	Ceramic capacitor, 0.5pF	ATC	100B 0R5
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infinion Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2K ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3K ohms	Digi-Key	P1.3KGCT-ND
R3	Chip resistor 2K ohms	Digi-Key	P2KECT-ND
R4	Potentiometer 2K ohms	Digi-Key	3224W-202ETR-ND
R5, R9	Chip resistor 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip resistor 1K ohms	Digi-Key	P1KECT-ND
R8	Chip resistor 5.1K ohms	Digi-Key	P5.1KECT-ND

**Gerber files for this circuit available on request*

Package Outline Specifications

Package H-30265-2

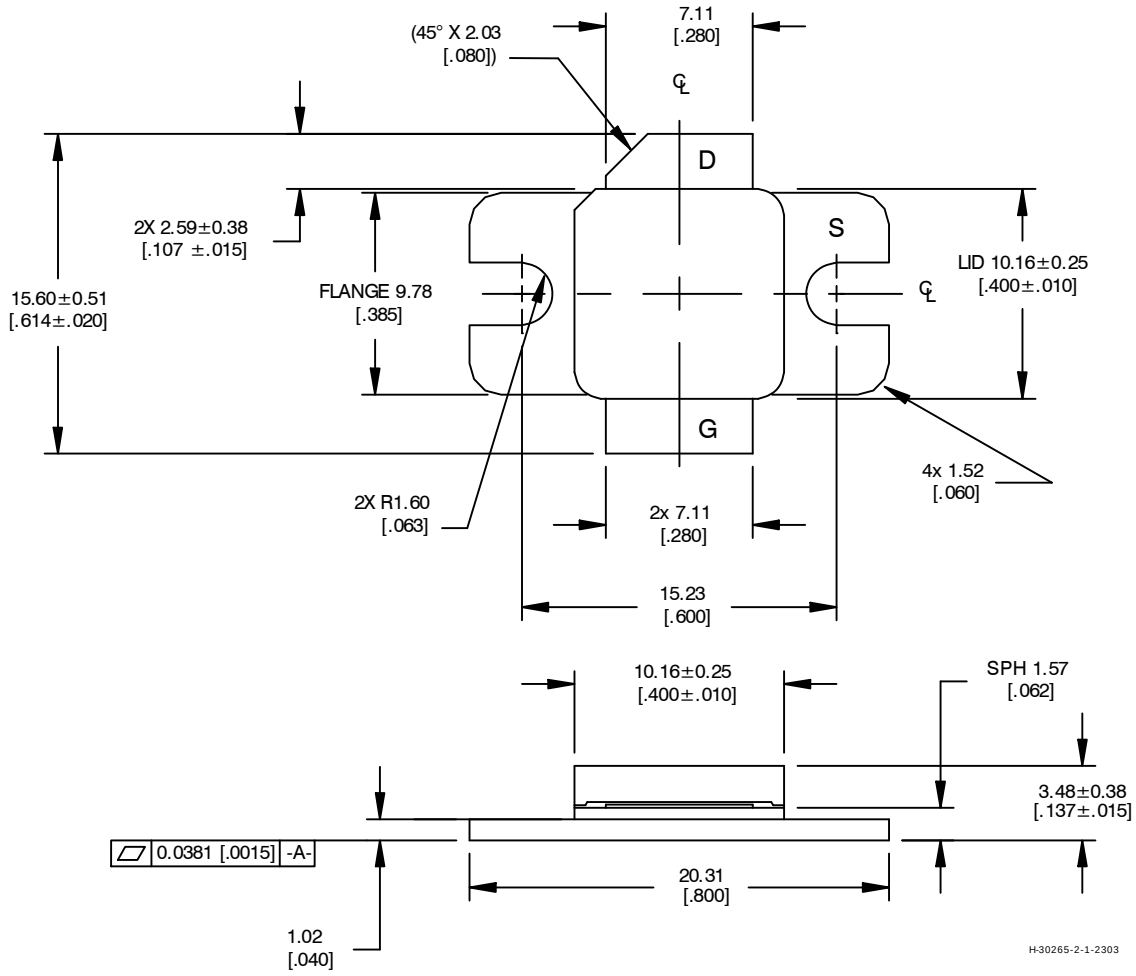


Diagram Notes—unless otherwise specified:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S - flange: 2.54 micron [100 microinch] (min)
   D, G - leads: 1.14 micron ± 0.38 micron [45 microinch ± 15 microinch] (min)

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Revision History:	**2008-03-17**	Data Sheet
Previous Version:	2006-11-10, Data Sheet	
Page	Subjects (major changes since last revision)	
all	Remove references to alternate Version 1.x products	

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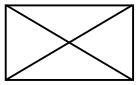

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